GLAST LAT ELECTRONICS SYSTEM - CONCEPTUAL DESIGN	Document # **LAT-DS-00226-D1**	Date Effective Draft 9/27/01
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Document Title **LAT VME Front-End Communication (Com) board – Conceptual Design**		

Gamma-ray Large Area Space Telescope (GLAST)
Large Area Telescope (LAT)
Conceptual Design of the LAT VME Front-End Communication (Com) board

DRAFT

Under Construction

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CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes

1 PURPOSE

This document describes the conceptual design for the LAT VME Front-End Communication (Com) board.

2 SCOPE

This document gives an overview over the conceptual architecture and implementation of the LAT VME Front-End Com board.

3 INTRODUCTION

The *GLAST* electronics system comprises many subsystems, which should be individually tested before system integration. Com board is designed to fill missing pieces for system test under software control.

Com board is designed for Simulation and Testing of GLAST electronic. It incorporate "pattern generator", in order to drive electronic with desired sequence of control and data signals, and " logic analyzer", in order to capture response of the system under test.

4 Requirements:

1. VME interface for CPU communication. Com board will support A32, D32 address space.
2. Simulate FE, TEM, GLT, and Controller card behavior. It should be able to reproduce control and data line behavior in response to internal or external trigger command
3. Record multiple real event from FE and TEM
4. Recognize trigger primitives and issue Trigger Acknowledgement in response to desired trigger primitives.

5 Implementation:

Block diagram of Com card implementation is represented on Figure 1.

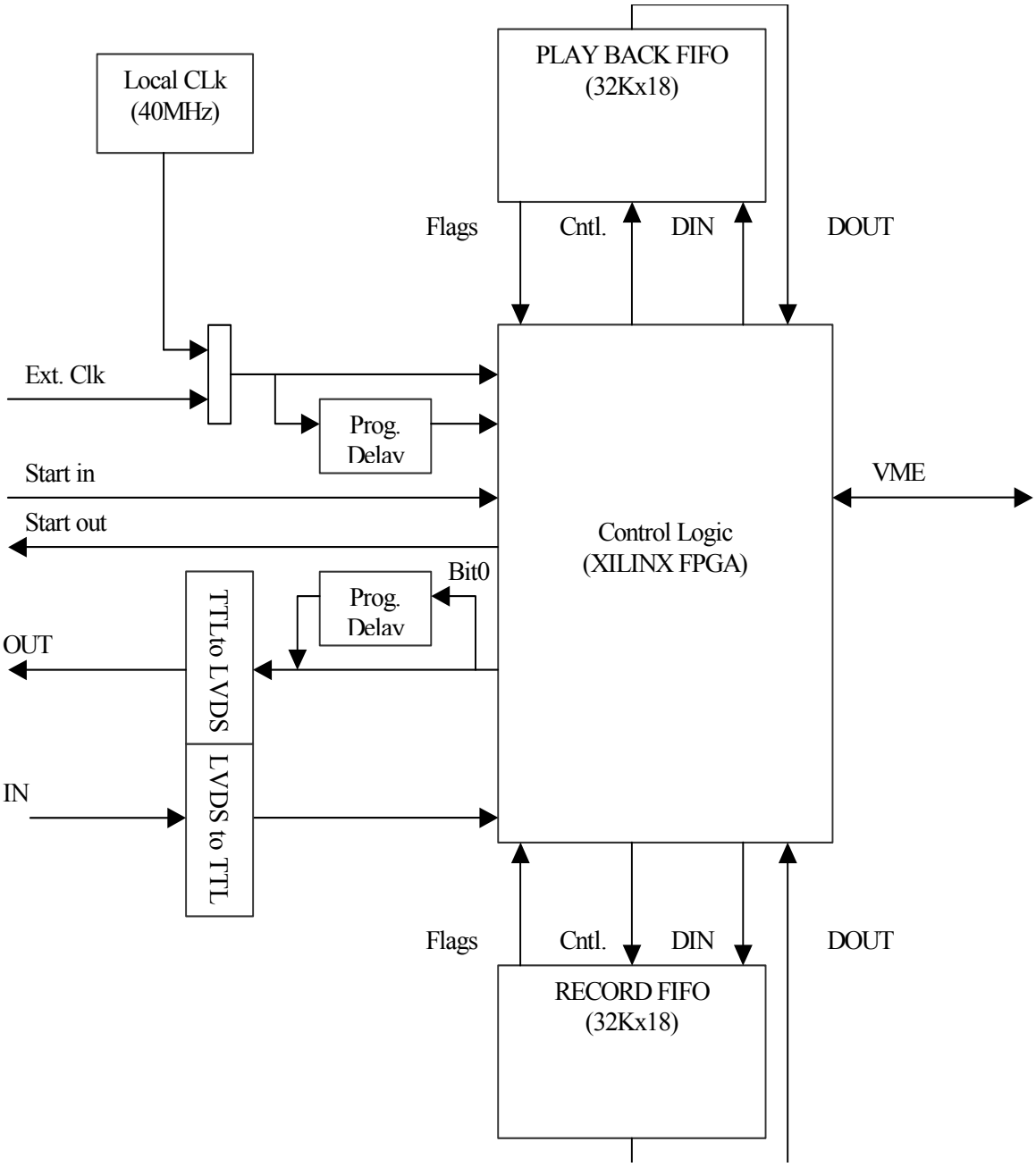

Figure 1:COM board block-diagram

1. VME interface support A32, D32 environment. It will support programmable (in hardware) interrupt in response to start of data recording after programmable delay.
2. Board can operate from internal or external clock, which is jumper selectable. Internal clock is run at twice of GLAST system clock at 40 MHz. External clock can be any frequency up to 50+MHz in order to check GLAST system margin from 0 to 25 MHz.
3. Board logic can operate at system clock frequency or system clock frequency divided by 2, which is control register selectable. Board use system clock to run FIFO logic when it run in pulse train mode on channel 0, which is clock output. In this mode channel 0 output is tied to FIFO channel 0

output. Or, board use system clock over two to run FIFO logic when it run in continues clock mode on channel 0. In this mode channel 0 output tied to continues clock at frequency equal system clock divided by two.

4. Implementation is using 32K deep PLAY BACK FIFO to implement desired control and data sequence in response to internal or external trigger command. It run at system clock or at system clock divided by 2 and can play up to 820 (1640) macro seconds. If biggest FIFO with same footprint is used it can play up to 6.5 (13.0) mSec. FIFO is configured by external CPU through XILINX interface. It is software configurable "pattern generator" which will take in account specific of the system under test.
5. Implementation is using 32K deep RECORD FIFO to record incoming events (DAQ requested the biggest 256K FIFO). The future version of the Com board will take multiple events of data if required. The current implementation will take one snapshot of data until FIFO is full. It start acquisition after some programmable delay when PLAY BACK FIFO start. Multi event implementation will decode start bit and event specific trailer (34 Zeros) for each event. This FIFO is used by software "logic analyzer" to check consistence of incoming events.
6. The future version will have option to decode trigger primitive(s) on desired channel(s) and respond to it with Trigger Acknowledgement signal on specified channel.
7. All signals are distributed as LVDS signal which is standard for GLAST communication.
8. Channel 0 of playback data has two additional features. Under configuration control in can output continues clock instead of PLAY BACK FIFO output at half of onboard clock frequency (20 MHz for internal clock source). Additionally, output of this channel can be skewed up to 60ns relatively to other channels in order exercise setup and hold time margin for electronic under test.
9. Incoming data clocked with programmably skewed clock in order to guaranty correct setup and hold time for incoming data
10. Each Com board will have 18 input and 18 output channels. Multiple Com boards can operate in the system by sourcing clock and start signals from one the board, which is selected as master.

6 VME Memory Map:

Memory space A32, D32. Board address selected by SW1 and SW2.

Registers:

1. Control
2. Status
3. Read FIFO data
4. Write FIFO data
5. Interrupt configuration

Control register: Base Address + 0x0

Bits	Function	R/W	Default
31	Start acquisition 0->1 Transition start acquisition	RW	0
30	Select source of start of acquisition, 0 – bit 31 start acquisition, 1 – external signal start acquisition	RW	0
29	Select between two modes of operation: 1. Programmable pulse train on channel 0. All board logic operated at system clock frequency. (0) 2. Continues clock on channel 0. All board logic operated at system clock/2 frequency (1)	RW	0
28-24	Unused	RW	0
23-16	Delay of write to Read-back FIFO for up to 6.4 uSec	RW	0
15	RECORD FIFO Partial reset (0 – reset), reset data, no conf.	RW	0
14	RECORD FIFO Master reset (0 – reset), reset data & conf.	RW	0
13	PLAY FIFO Partial reset (0 – reset), reset data, no conf.	RW	0
12	PLAY FIFO Master reset (0 – reset), reset data & conf.	RW	0
11-6	Read-back clk delay in 2ns steps. Maximum delay is 60ns	RW	0
5-0	Channel 0 delay in 2ns steps. Maximum delay is 60ns	RW	0

Figure 2: Control Register

Transmit of data will not start unless record (write) FIFO is not empty up to PAE flag (511 word in FIFO).

Each data tacking will fill RECORD FIFO up to Full flag.

Playback will play data until PLAY FIFO is empty.

Playback data will stay in FIFO until FIFO is reset or new data is overwritten on top of them. Start signal will play same data over and over again without reloading of Playback FIFO.

Last read data will stay on output bus until new playback overwrite it.

Programmable flags configured to 511 words away from empty or full.

FIFO should be out of reset in order to have normal operation (bits 15-12)

Status register: Base Address + 0x4

Bits	Function	R/W	Default
31-29	Hardware version	R	0x1
28-26	Hardware revision	R	0x1
25-23	Software version	R	0x1
22-20	Software revision	R	0x1
19-17	Unused	R	0
16	System in run state – current value	R	0
15	Play back FIFO programmable Almost Empty Flag(511) – latched value	RW	0
14	Play back FIFO programmable Almost Full Flag(Full –511) – latched value	R(W –1 reset)	0
13	Play back FIFO Empty Flag – latched value	R(W –1 reset)	0
12	Play back FIFO Full Flag – latched value	R(W –1 reset)	0
11	Write FIFO programmable Almost Empty Flag (511) – latched value	R(W –1 reset)	0
10	Record FIFO programmable Almost Full Flag(Full – 511) – latched value	R(W –1 reset)	0
9	Record FIFO Empty Flag – latched value	R(W –1 reset)	0
8	Record FIFO Full Flag – latched value	R(W –1 reset)	0
7	Play back FIFO programmable Almost Empty Flag(511) – current value	R	0
6	Play back FIFO programmable Almost Full Flag(Full – 511) – current value	R	0
5	Play back FIFO Empty Flag – current value	R	0
4	Play back FIFO Full Flag – current value	R	0
3	Record FIFO programmable Almost Empty Flag(511) – current value	R	0
2	Record FIFO programmable Almost Full Flag(Full – 511) – current value	R	0
1	Record FIFO Empty Flag – current value	R	0
0	Record FIFO Full Flag – current value	R	0

Figure 3: Status register

Play back FIFO register: Base Address + 0x8

Bits	Function	R/W	Default
31-18	N/A	-	0
17-0	Data	RW	0

Figure 4: Play back FIFO

Record FIFO flags register: Base Address + 0xC

Bits	Function	R/W	Default
31-18	N/A	-	0
17-0	Data	RW	0

Figure 5: Record FIFO

Interrupt Configuration: Base Address + 0x10

Bits	Function	R/W	Default
31-19	Delay of interrupt after start of write to Read-back FIFO in 0.8(1.6) uSec steps. Up to 6.5(13.0) mSec total delay*	RW	0
18-16	Interrupt IRQ level. Board designed to implement the following priority IRQ2, IRQ3, IRQ4, IRQ5. Board does not do anything if IRQ1,IRQ6,IRQ7 selected	RW	0
15-0	Interrupt vector	RW	0

Figure 6: Interrupt Configuration Register

*The first number for pulse train operation, the second number for continues clock operation.

Interrupt logic implement ROAK (Release On Acknowledge) logic. And output interrupt vector programmed in Interrupt Configuration Register.

7 Board interfaces:

J #	Connector type	
	Connector on PCB	Documentation
J1	3M-100 male right angle wall condo header, part# 3433-D302 (2 50pin ribbon cable connectors together)	3M Catalog
J3	LEMO, part# EPY.00.250.NTN (2 LEMO connectors)	LEMO Catalog
J4	LEMO, part# EPY.00.250.NTN (2 LEMO connectors)	LEMO Catalog
J5	LEMO, part# EPY.00.250.NTN (2 LEMO connectors)	LEMO Catalog
J6	LEMO, part# EPL.00.250.NTN (1 LEMO connectors)	LEMO Catalog
J7	LEMO, part# EPL.00.250.NTN (1 LEMO connectors)	LEMO Catalog
J9	Johnson components, part#142-0701-501 (SMA connector)	Johnson SMA Catalog PC Mount section

Figure 7: Connector type

Row number (starting from bottom)	Signal name on J1			
	Column 0 (next to PCB)	Column 1	Column 2	Column 3
Row 0	Out0-	Out0+	In0-	In0+
Row 1	Out1-	Out1+	In1-	In1+
Row 2	Out2-	Out2+	In2-	In2+
Row 3	Out3-	Out3+	In3-	In3+
Row 4	Out4-	Out4+	In4-	In4+
Row 5	Out5-	Out5+	In5-	In5+
Row 6	Out6-	Out6+	In6-	In6+
Row 7	Out7-	Out7+	In7-	In7+
Row 8	Gnd	Gnd	Gnd	Gnd
Row 9	Gnd	Gnd	Gnd	Gnd
Row 10	Out8-	Out8+	In8-	In8+
Row 11	Out9-	Out9+	In9-	In9+
Row 12	Out10-	Out10+	In10-	In10+
Row 13	Ou11-	Out11+	In11-	In11+
Row 14	Out12-	Out12+	In12-	In12+
Row 15	Out13-	Out13+	In13-	In13+
Row 16	Out14-	Out14+	In14-	In14+
Row 17	Out15-	Out15+	In15-	In15+
Row 18	Gnd	Gnd	Gnd	Gnd
Row 19	+2.5V digital (can be changed to +3.3V, change R3 to 200 Ohm)	+1.5V analog	+12V	Gnd
Row 19	+150V analog (has to supplied to board)	+2.5V analog(can be changed to +3.3V, change R6 to 200 Ohm)	-12V	+5V
Row 20	Ou16-	Out16+	In16-	In16+
Row 21	Ou17-	Out17+	In17-	In16+
Row 22 (signals unused)	Ou18-	Out18+	In18-	In19+
Row 23(signals unused)	Ou19-	Out19+	In19-	In19+

Figure 8: Signals on J1 connector

J #	Signal name	
	Connector next to PCB	Connector away from PCB
J3	Start_out	Start_in
J4 (unused)	Test 1	Test 0
J5	+2.5V analog	+1.5V analog
J6	150V (need external source)	-
J7	+2.5V analog	-
J9	External clock (H3 select between internal and external clock)	-

Figure 9: Signals on J3-J9 connectors

D #	LED name	
	Connector next to PCB	Connector away from PCB
D1	VME – indicate VME access	RUN – indicate active state of playback and record data

Figure 10: LED

SW#	Position #	Board Address configuration (0 – "on" position, 1 – "off" position"
		Address line
SW1	0	A31
	1	A30
	2	A29
	3	A28
	4	A27
	5	A26
	6	A25
	7	A24
SW2	0	A23

	1	A22
	2	A21
	3	A20
	4	A19
	5	A18
	6	A17
	7	A16

Figure 11: Board address configuration